Section 7

Chapter 4

SEMICONDUCTOR MANUFACTURING

by

M.K. Carol Lee, P.E.

and

J. Julian Elliot, P.E.

Revision 2.0

ACKNOWLEDGEMENT

The authors acknowledge the significant contributions of the following members of the Semiconductor Workgroup:

Tom Cooper, Intel
Diana Garcia, National Semiconductor
Linda Gee, LSI Logic
Carol Knowles, Advanced Micro Devices
Jenna Latt, Advanced Micro Devices
Trang Mary Le, Intel
John Marvin, Bay Area Air Quality Management District
Thomasina Mayfield, Bay Area Air Quality Management District
Scott Nixon, Hewlett-Packard
Lynne Reardon, Hewlett-Packard
Diane Van Schoten, Philips
Joe Slamovich, Bay Area Air Quality Management District
Gene Willner, Bay Area Air Quality Management District

TABLE OF CONTENTS

I. PROCESS DESCRIPTIONS

Semiconductor manufacturing refers to the series of manufacturing processes, which produce packaged integrated circuits (ICs). Most packaged ICs are assembled onto printed circuit boards (PCBs) by a separate manufacturer. However, some packaged ICs, such as microprocessor upgrades and memory modules, are used without pre-assembly onto a circuit board. PCB assembly is the subject of a separate Permit Handbook chapter.

This section provides basic information about semiconductor manufacturing processes and their emissions and permitting requirements, as summarized in Table 1 (Blank Wafer Production), Table 2 (Semiconductor Fabrication), and Table 3 (Assembly and Packaging). The manufacturing process includes the major steps shown in Figure 1 (Semiconductor Manufacturing Process). The guidelines in this chapter may also apply to non-semiconductor fabrication operations, which use similar manufacturing technologies. In accordance with Regulation 2-1-231, semiconductor fabrication does not include crystal growth, circuit separation and encapsulation operations.

The semiconductor manufacturing processes may be divided into three major categories:

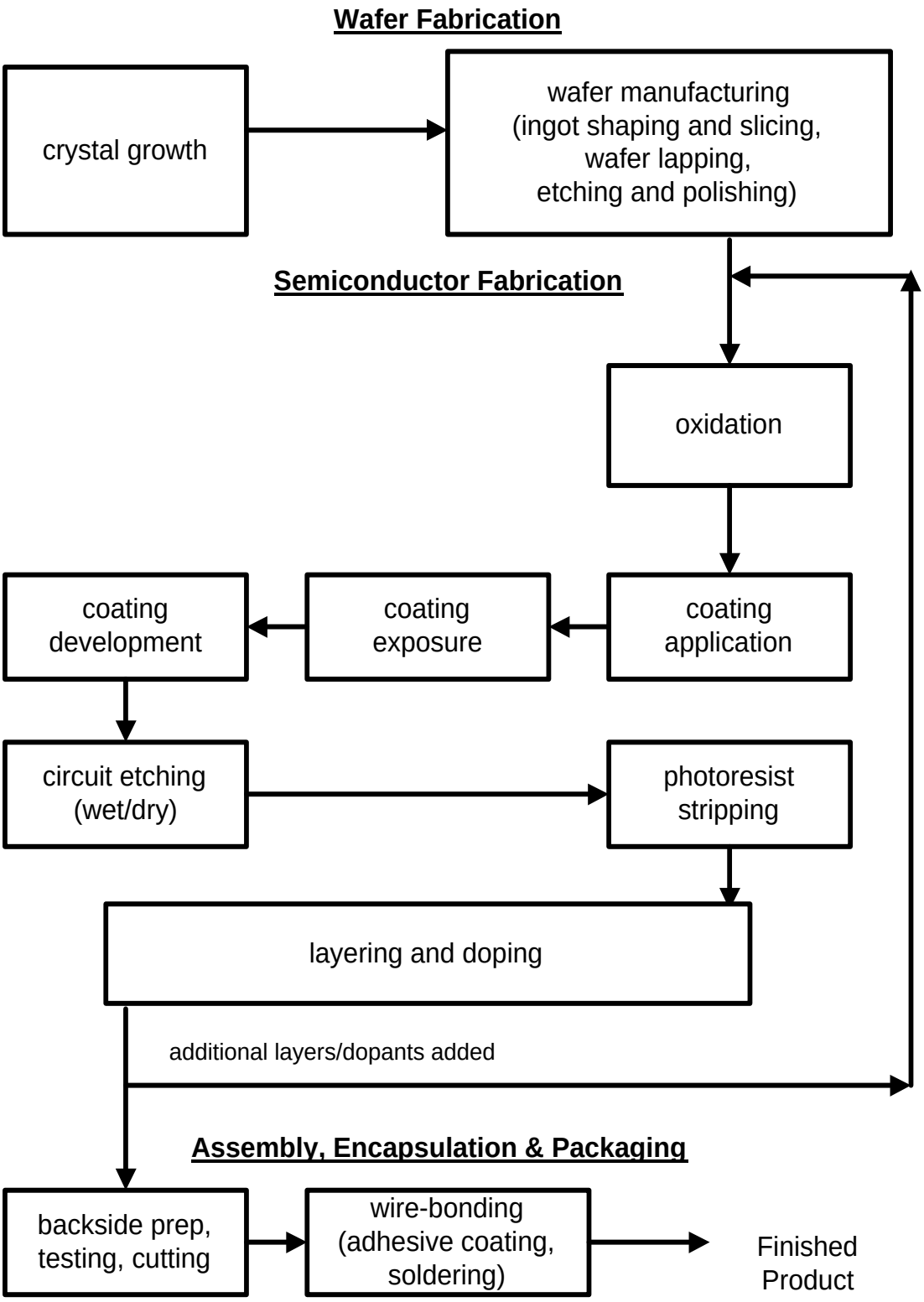
A. Blank wafer production, **where blank wafers are produced, usually at dedicated facilities which perform no semiconductor fabrication or packaging.**

B. Semiconductor fabrication, **where integrated circuits (ICs) are produced on the wafers.**

C. Assembly and packaging, **where the wafers are cut into individual ICs which are then mounted into a package for assembly on a printed circuit board.**

Semiconductor wafers may be made from a variety of substrates. The most common is silicon; others include gallium arsenide (GaAs) and indium phosphide (InP). In general, all substrates will have the same processing steps and similar emissions of regulated pollutants (POC, NPOC. PM_{10}). However, different substrates require the use of different processing materials for etching, doping, and layering operations (discussed below), resulting in different hazardous air pollutant (HAP) emissions.

Although the following discussion focuses on silicon substrate processing, the permitting guidelines and emission calculation methods are applicable to any substrate.



During semiconductor fabrication, wafers undergo cleaning and chemical mechanical polishing throughout the process.

FIGURE 1 - SEMICONDUCTOR MANUFACTURING PROCESS

A. Blank Wafer Production

1. Silicon Crystal Growth

Molten silicon is introduced into a mold with a seed crystal of silicon. As the molten silicon cools, it crystallizes around the seed to "grow" a single crystalline ingot. Crystal growth is not in itself a source of air emissions and is not subject to permit requirements.

Miscellaneous cleaning operations may result in organic or inorganic emissions. Organic cleaning operations may be exempt in accordance with Regulation 2-1-118. Abatement of organic or inorganic emissions may be required if emissions exceed the current best available control technology (BACT) trigger level.

2. Wafer Manufacturing

The cooled silicon ingot is shaped and sliced into round wafers which are mechanically polished ("lapped"). These steps are subject to the particulate emission limits of Regulation 6 if particulate emissions are produced and vented outside of the facility. Mechanical shaping, slicing and polishing may be exempt from permit requirements in accordance with Regulation 2-1-121.1 or 2-1-125.1.2.

After polishing, wafers are etched in a chemical bath to remove surface imperfections. Depending on the type and concentration of etchants used, mists and aerosols may be produced. Finally, each wafer is polished to a smooth finish. The etching operations may be exempt from permitting requirements by Regulation 2-1-127.4, if the toxic risk provisions of Regulation 2-1-316 are satisfied.

If adhesives are used to fix wafers in position during polishing, the use of adhesives may be subject to VOC limits and other requirements in Regulation 8, Rule 51. The application of adhesives may be exempt from permit requirements in accordance with Regulation 2-1-119.2, if the toxic risk provisions of Regulation 2-1-316 are satisfied. Miscellaneous cleaning operations may result in organic or inorganic emissions. Organic cleaning operations may be exempt in accordance with Regulation 2-1-118. Abatement of organic or inorganic emissions may be required if emissions exceed the current best available control technology (BACT) trigger level.

B. Semiconductor Fabrication

1. Overview

The processes used to form ICs on the wafer, as illustrated in Figure 1, include:

- Oxidation, where an inert layer of silicon dioxide is formed on the wafer by exposing the wafer to a heated oxygen environment.
- Photoresist application, exposure and development, where solvent-based, light-sensitive resin solutions are uniformly applied to the wafer and then processed to leave a pattern of cured photoresist on the wafer which corresponds to the circuit image, while removing the non-image coating. Photoresist applicators may also apply non-light sensitive coatings (spin-on-glass, anti-reflective coatings) and solvents (edge bead remover, hexamethyldisilazane (HMDS)).
- Etching, where reactive gases or liquids are used to remove the silicon dioxide layer from the wafer surface where it is not protected by cured photoresist, thereby exposing the underlying silicon for further processing; liquid etching is classified as a wet chemical station, as described below.

- Photoresist stripping, where cured photoresist is removed from the wafer after it has allowed selective wafer surface processing; stripping solutions may be organic or inorganic depending on the composition of the underlying wafer surface, and therefore may be classified as either solvent stations or a wet chemical stations, as described below.
- Doping (diffusion, ion implant), where the wafer is exposed to impurities which penetrate into the exposed silicon patterns to selectively modify the electrical conductivity of the silicon, thereby producing electronic components and circuits.
- Layering (epitaxial growth, metallization films, chemical vapor deposition), where a doped wafer is covered with a uniform layer of silicon (to form a base for additional circuit layers) or metal (to form a conductive connection between the circuit layers and the external IC package).

Other processes include:

- Chemical mechanical polishing (CMP), where wafer surfaces are polished to maintain wafer flatness during processing.
- Solvent stations, where wafers or tools are cleaned by immersion in a solvent liquid or vapor or by being sprayed with a solvent liquid.
- Wet chemical stations, where wafers or tools are cleaned or etched by immersion in an inorganic solution or by being sprayed with such a solution.
- Wipe cleaning, where tools and work surfaces are cleaned in place or at a dedicated station.

2. Detailed Process Descriptions

a. Oxidation

Silicon wafers are exposed to oxygen at high temperature to form a layer of silicon dioxide on the wafer surface. This layer is selectively removed in subsequent processing steps, allowing the underlying silicon to be modified in a pattern, which corresponds to electronic components and circuits. The oxygen source used in oxidation may either be steam (wet oxidation) or oxygen (dry oxidation).

Oxidation is not itself a source of air emissions and is not subject to permit requirements. However, sometimes a chlorine source (chlorine gas, hydrochloric acid, trichloroethylene or trichloroethane) is used during oxidation to modify the oxide characteristics. Oxidation furnaces may also be cleaned with chlorine vapor. Standard industry practice is to abate oxidation chambers with wet or dry scrubbers.

b. Coating Application

Photoresist is a solution of light-sensitive resin and solvent, which is applied on a "spin track." Modern spin tracks are integrated tools where a variety of different materials (photoresist, edge bead remover, spin-on-glass, etc.) may be applied. On the spin track, a fixed amount of photoresist is metered onto the wafer, which is then spun at high speed on a rotating element to uniformly coat the wafer surface. Some of the photoresist applied on the spin track is flung from the wafer into the spin track tool and recovered as waste. The coated wafer is then heated to evaporate photoresist solvent, either on the spin track tool or in a separate oven. Therefore, all of the solvent in the photoresist, which

remains on the wafer, is emitted, and some portion of the solvent in the excess photoresist may also be emitted depending on the design of the spin track and waste collection system. Spin-on-glass and other coatings and edge bead remover are applied in the same way. Spin-on-glass is a non-light-sensitive coating which acts as a protective layer or which provides a good adhesive surface for subsequent layers. Edge bead remover is a solvent, which is spun onto a coated wafer to remove the photoresist bead, which forms on the outside edge of a coated wafer. HMDS may be applied to a wafer to improve adhesion of subsequent coating layers.

Spin tracks may utilize automatic cleaning where solvent, typically isopropyl alcohol (IPA), acetone, or propylene glycol methyl ether acetate (PGMEA), is dispensed onto the spin track to prevent photoresist buildup. Manual wipe cleaning of spin tracks is also regularly performed, typically with an IPA solution.

Coating application equipment may be required to be abated if total fab area emissions exceed the current best available control technology (BACT) trigger level. Spin tracks where solvent-based developer photoresist is applied may be required to be abated in accordance with Regulation 8-30-302.

c. Photoresist Exposure

After a wafer has been coated with photoresist and the photoresist has been cured, the wafer is exposed to a light source through a template called a "mask." The mask is a glass plate on which an image of the circuit has been produced. Exposing a wafer through the mask causes a portion of the photoresist coating, corresponding to the circuit image, to react. "Positive photoresist" will soften relative to the unexposed photoresist. "Negative photoresist" will harden relative to unexposed photoresist. Then, depending on which type of photoresist is used, either the image or non-image portion of the photoresist is removed in a photoresist developer as described below.

Because photoresist solvent is evaporated during application and curing, exposure of coated wafers does not result in additional emissions and exposure equipment does not require a permit.

Some equipment associated with exposure, such as the masks, may require solvent cleaning, typically in a solvent station as described below. Solvent stations may be required to be abated if total fab area emissions exceed the current best available control technology (BACT) trigger level.

d. Photoresist Development

Development is the process of removing soft photoresist on the wafer (either the image or non-image portion depending on the type of photoresist used) to expose a portion of the silicon dioxide layer corresponding to the circuit image. Development may be performed on spin tracks, in sinks, or in enclosed spray units. Negative photoresists may use organic or exempt inorganic developer solutions.

Developer emissions from organic developers are similar to photoresist emissions when development is performed on a spin track. When sinks or

enclosed units are used, emissions are similar to those from solvent stations, as described below.

Photoresist developers may be required to be abated if total fab area emissions exceed the current best available control technology (BACT) trigger level. Spin tracks or spray units where solvent-based developer is applied may require abatement in accordance with Regulation 8-30-302.

e. Wet Etching

Wet etching is the process of removing exposed silicon dioxide in the pattern created by photoresist exposure and development with a liquid, typically an inorganic acid. Wet etchers are classified as wet chemical stations and may be exempt from permit requirements in accordance with the criteria for wet chemical stations.

Abatement of wet chemical stations may be required if etcher emissions exceed the current best available control technology (BACT) trigger level.

Standard industry practice is to abate wet chemical stations at wet scrubbers.

f. Dry Etching

In dry etching, reactive gas plasma is used in place of a wet etching solution. Dry etching provides a higher resolution than wet etching and therefore is more likely to be used as circuit elements become smaller. Dry etching generally produces less "undercutting" of the wafer substrate under photoresist, often provides more control over etching rate, and may be necessary where the etched layer is resistant to liquid etchants. Gaseous etching is generally performed with halogenated compounds which, depending on the wafer substrate, may be bromine, chlorine, fluorine or iodine-based gases in a carrier gas (Reference 1). Some of these etchants may be HAPs. Also, plasma operations will break the halogenated compounds into related compounds. For example, use of chlorine (Cl_2) plasma with a hydrogen carrier will produce chlorine and hydrochloric acid (HCl) emissions. Standard industry practice is to abate dry etchers at wet scrubbers.

g. Photoresist Stripping

After etching, the remaining photoresist on the wafer is removed in a photoresist stripper. Photoresist strippers are classified as solvent stations if they use organic solvents, or wet chemical stations if they use acids or hydrogen peroxide solutions. Strippers may be exempt from permit requirements in accordance with the criteria for wet chemical stations and solvent stations. Strippers have a variety of physical designs, ranging from manual or automated dip sinks to more sophisticated units where wafers are immersed in or sprayed with stripper solution.

Abatement of strippers may be required if total fab area emissions exceed the current best available control technology (BACT) trigger level.

Standard industry practice is to abate strippers, which use inorganic solutions at wet scrubbers.

h. Doping - Diffusion

Doping is performed through diffusion by either exposing the wafer to a high temperature environment of dopant vapor in a carrier gas (gaseous diffusion), or by covering the surface which is to be doped with a temporary layer of dopant oxide (non-gaseous diffusion). The most common dopants include arsenic, boron and phosphorus. Others include aluminum, antimony, beryllium, gallium, germanium, gold, magnesium, tellurium and tin.

Dopant gases such as arsine, silane, phosphine and diborane are highly toxic. All of these gases, except arsine, are also "pyrophoric" - igniting on contact with atmospheric oxygen. Silane has the property of forming silica particles when ignited. Standard industry practice is to vent pyrophoric gases to chambers where they are ignited under controlled conditions, and then vented to wet scrubbers, and to abate non-pyrophoric gases at wet scrubbers.

i. Doping - Ion Implantation

Ion implantation provides a more controlled doping mechanism than diffusion. In ion implantation, dopant material is ionized in a vacuum chamber, then accelerated and imbedded into the wafer with an implanter. Standard industry practice is to abate ion implanters at combustion chambers (when pyrophoric gases are used) and wet scrubbers.

j. Layering - Epitaxial Growth

Epitaxial growth is the process of re-establishing a fresh silicon layer on a wafer using exposed silicon on the wafer surface as a seed for additional silicon crystal growth. Epitaxial growth occurs in an epitaxial reactor (or "siliconizing reactor") where the wafer is exposed to silane and dopant gases in a high temperature environment. Silicon layer growth is also performed with molecular beam epitaxy (MBE), in which silicon and dopants are evaporated and deposited on the wafer in a vacuum environment. Standard industry practice is to abate epitaxial growth processes at combustion chambers with wet scrubbers.

k. Layering - Sputtering

Sputtering is the process of impinging ionized gas atoms, typically argon, on a metal target in order to generate microscopic metal fragments which are deposited on the wafer as a thin film. Sputtered metals include titanium, platinum, gold, molybdenum, tungsten, nickel and cobalt. Standard industry practice is to abate sputtering chambers at wet scrubbers.

l. Layering - Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a process in which a metal or silicon compound is vaporized and deposited onto the wafer as a thin film. Some CVDs are operated with a vacuum environment. Standard industry practice is to abate exhaust gases from CVD chambers at wet scrubbers.

m. Chemical Mechanical Polishing

Chemical mechanical polishing (CMP) is a polishing step performed after layering or other coating processes in order to re-establish the wafer flatness required for subsequent processing steps. Standard industry practice is to vent CMP tool exhaust to wet scrubbers.

n. Solvent Stations

Solvent station refers to any process used to clean wafers or remove photoresist from wafers with an organic solvent solution (excluding developer solutions applied at spin tracks which are classified as developers), as well as processes used to clean tools (excluding manual wipe cleaning). However, for consistency with Regulation 2-1-118.4 and 118.5, only processes which use unheated solutions with 10 weight percent VOC or more or heated solutions with 2.5 weight percent VOC or more should be considered solvent stations; processes which use lower-VOC solutions should be considered wet chemical stations. The most common organic solvents used in solvent stations are isopropyl alcohol (IPA), acetone and n-methyl pyrrolidone (NMP). Abatement of solvent stations may be required if total fab area emissions exceed the current best available control technology (BACT) trigger level.

o. Wet Chemical Stations

Wet chemical station refers to any process in which inorganic solutions are used to clean or etch wafers, or to clean tools. Inorganic solutions include caustic or acidic solutions as well as unheated organic solutions with less than 10 weight percent VOC and heated solutions with less than 2.5 weight percent VOC. Some wet chemical stations, such as wet etchers, may use air-agitation of solutions to increase or control the etching rate.

Wet chemical stations are a more complex permitting problem than solvent stations. Many materials used in wet chemical stations are classified as HAPs. Some of these materials produce odorous or irritating fumes in the form of PM_{10} emissions. The table below lists some common wet chemical station chemicals (Reference 1, 2):

Material	*Properties*
Aqua regia (nitrohydrochloric acid), hydrochloric acid, hydrofluoric acid, nitric acid ("fuming"), sulfuric acid ("fuming", "oleum")	Fuming acids which generate irritating PM_{10} aerosols; aqua regia, hydrochloric acid, hydrofluoric acid and nitric acid are HAPs
Ammonia, ammonium hydroxide, phosphoric acid	HAPs, irritants
Hydrogen peroxide, acetic acid	Irritants

p. Tool / Fab Wipe Cleaning

Like wafers, tools may be cleaned at solvent and wet chemical stations. Wipe cleaning refers to manual wipe cleaning of work surfaces or tools which is performed either in-place or at a dedicated cleaning station. Wipe cleaning may be exempt from permit requirements in accordance with Regulation 2-1-118.4, 2-1-118.5 or 2-1-118.9, if the toxic risk provisions of Regulation 2-1-316 are satisfied. Guidance on the permitting and evaluation of wipe cleaning operations is provided in a separate permit handbook chapter. Abatement of manual wipe cleaning may be required if total fab area emissions exceed the current best available control technology (BACT) trigger level.

C. Assembly and Packaging

After circuit production is complete, the non-circuit wafer side is mechanically milled down to improve heat dissipation and reduce the possibility of breakage ("backside prep"). After each IC on the wafer is tested, the individual ICs on the wafer are cut apart.

During "wire-bonding" the IC is mounted in a ceramic or metal package, or in metal lead frames that will be encapsulated in plastic. Wires are soldered between connection points on the IC and leads on the mounting package or lead frame.

Wafer processing during backside prep, testing, cutting, and wire-bonding is exempt from permit requirements in accordance with Regulation 2-1-113.2.12 and 2-1-126.2 (for backside prep, testing), 2-1-121.1 or 2-1-125.1.2 (for cutting) and 2-1-128.11 (for wire bonding), if the toxic risk provisions of Regulation 2-1-316 are satisfied.

Assembly and packaging wipe cleaning may be exempt in accordance with Regulation 2-1-118.4, 2-1-118.5 or 2-1-118.9, if the toxic risk provisions of Regulation 2-1-316 are satisfied. The application of adhesives and other coatings may be exempt from permit requirements in accordance with Regulation 2-1-119.2, if the toxic risk provisions of Regulation 2-1-316 are satisfied. Guidance on the permitting and evaluation of these processes, as well as printed circuit soldering operations, is provided in other permit handbook chapters.

Abatement of these other operations may be required if estimated emissions exceed the current best available control technology (BACT) trigger level. These emissions are considered separately from blank wafer production and semiconductor fabrication processes.

D. Miscellaneous Operations

Chemical handling and laboratory operations may be found in any of the three categories of semiconductor manufacturing processes. Chemical handling, including preparation of reagents and distribution of solvents from bulk containers, should be assumed to be exempt by Regulation 2-1-103. Laboratory operations, including failure analysis and quality assurance testing, may be exempt by Regulation 2-1-113.2.12 or 2-1-126.2.

TABLE 1 - BLANK WAFER PRODUCTION SUMMARY

Process / Emissions	*Permit Requirement*	*Abatement Requirement*	*Record Requirement*
Silicon crystal growth	No (negligible emissions)	None	None
Ingot shaping	No, if exempt[2] by 2-1-121.1 or 2-1-125.1.2	As required to comply with 6-300	None
Wafer slicing and polishing	No, if exempt[2] by 2-1-121.1 or 2-1-125.1.2	As required to comply with 6-300	None
Adhesive application	Yes (Data Form S) [potentially exempt[2] by 2-1-119.2]	8-51-302, BACT	8-51-500, Permit conditions
Inorganic processing equipment	No, if exempt[2] by 2-1-118.4, 2-1-118.5, 2-1-118.6, 2-1-118.7 or 2-1-127.4	None, if exempt from permit requirements	None
Solvent cleaning equipment	YES (Data Form S & SC)[1] [potentially exempt[2] by 2-1-118.4, 2-1-118.5, 2-1-118.6 or 2-1-118.7]	8-16-300 BACT (Data Form A, C, P)[3]	8-16-500, Permit conditions
Wafer etching	No, if exempt b 2-1-127.4	None, if exempt from permit requirements	
Manual wipe cleaning	YES (Data Form S)[1] [potentially exempt[2] by 2-1-118.4, or 2-1-118.5, or 2-1-118.9]	BACT (Data Form A, C, P)[3]	8-16-500 Permit conditions

*

1 Form P-101B (Application for Authority to Construct, Permit to Operate, or Banking) should be completed and submitted with any new application (one form per application).

2 Equipment is exempt from the requirements of Section 2-1-301 and 2-1-302 provided it is not subject to any of the requirements of 2-1-316 through 318.

3 Forms A, C, and P are only required if applicable. Form A, C, and P should be used for thermal oxidizers and other abatement devices which combust fuel. Form A and P should be used for scrubbers.

TABLE 2 - SEMICONDUCTOR FABRICATION SUMMARY

Process / Emissions	*Permit Requirement*	*Abatement Requirement*	*Record Requirement*
Semiconductor Fabrication Area	YES (Data Form F Worksheet) [1] [potentially exempt by 2-1-124]	8-30-300, BACT (Data Form A, C, P)[3]	8-30-500
Tool solvent cleaning (subject to Regulation 8-16)	YES (Data Form S & SC)[1] [potentially exempt[2] by 2-1-118.4, or 2-1-118.5, or 2-1-118.6, or 2-1-118.7]	8-16-300, BACT (Data Form A, C, P)[3]	8-16-500, Permit conditions
Manual wipe cleaning	Included in fab area (Data Form F Worksheet)[1] [potentially exempt[2] by 2-1-118.4, or 2-1-118.5, or 2-1-118.9]	BACT (Data Form A, C, P)[3]	8-16-500, Permit conditions

*

Footnotes 1, 2, 3 explained after Table 1 or 3.

TABLE 3 - ASSEMBLY, ENCAPSULATION AND PACKAGING SUMMARY

Process/Emissions	*Permit Requirement*	*Abatement Requirement*	*Record Requirement*
Backside prep - adhesive application	YES (Data Form S)[1] [potentially exempt[2] by 2-1-119.2]	8-51-300, BACT (Data Form A, C, P)[3]	8-51-500, Permit conditions
Solvent cleaning (tools and finished ICs and IC packages)	YES (Data Form S & SC)[1] [potentially exempt[2] by 2-1-118.4, or 2-1-118.5, or 2-1-118.6, or 2-1-118.7]	8-16-300, BACT (Data Form A, C, P)[3]	8-16-300, 8-30-300, Permit conditions
Manual wipe cleaning	YES (Data Form S)[1] [potentially exempt[2] by 2-1-118.4, or 2-1-118.5, or 2-1-118.9]	BACT (Data Form A, C, P)[3]	Permit conditions

1

1 Form P-101B (Application for Authority to Construct, Permit to Operate, or Banking) should be completed and submitted with any new application (one form per application).

2 Equipment is exempt from the requirements of Section 2-1-301 and 2-1-302 provided it is not subject to any of the requirements of 2-1-316 through 318.

3 Forms A, C, and P are only required if applicable. Form A, C, and P should be used for thermal oxidizers and other abatement devices which combust fuel. Form A and P should be used for scrubbers.

II. FABRICATION AREA PERMIT GUIDELINES

A. What is a Fab Area?

The semiconductor fabrication area ("fab area") permit structure is unique to semiconductor fabrication facilities and allows multiple pieces of equipment which require permits to be grouped as a single source. In a fab area source, usage of organic and toxic materials are tracked, but individual equipment or device information and their quantity are not. This permit structure is used because semiconductor fabrication may require a very large number of individual devices to make one product. Also, unlike other facilities, semiconductor fabrication facilities are allowed to add or replace individual devices with functionally equivalent devices without a permit modification as long as there is no increase in solvent throughput and/or criteria or toxic emissions.

B. What equipment may be permitted as part of a Fab Area?

At semiconductor fabrication facilities, virtually all equipment should be included in a fab area source, except for non-wafer solvent cleaning devices, such as vapor degreasers and large cold cleaners, which are subject to Regulation 8, Rule 16. In addition, in accordance with Regulation 2-1-231, semiconductor fabrication does not include crystal growth, circuit separation and encapsulation operations. Equipment at blank wafer production facilities and assembly and packaging facilities should not be grouped into fab area sources.

However, solvent sinks which are subject to Regulation 8, Rule 30 may be included in a fab area, even if used to clean tools and not wafers. Ancillary devices such as boilers and bulk solvent storage tanks should not be included in fab area permits; solvent reservoirs, which are part of tools do not require individual permits.

C. How is equipment distributed into Fab Area permits?

In general, equipment at semiconductor fabrication facilities may be distributed into fab area sources as desired by the applicant. For example, all facility equipment may be grouped into a single fab area, or multiple fab areas may be established to correspond to product lines or clean room environments. However, it is preferable to not have a single fab area source with a large number of sources which are distributed over a large physical area, such as multiple buildings, since inspection of such a source would be unwieldy. Also, a single product line which would normally be considered a single fab area should not be divided into smaller fab areas or individual sources for the purpose of circumventing BACT requirements or other requirement which are triggered on a source-specific basis.

D. When may Fab Area equipment be replaced without a permit?

Equipment permitted as part of a fab area may be replaced with another device of the same type without a permit application as described in Regulation 2-2-223. If the replacement requires a change to permit conditions, such as an increase in permitted emissions or throughput, then a permit application is required.

E. What is Best Available Control Technology (BACT) for Semiconductor Fabrication Operations?

The District's BACT/TBACT Workbook specifies BACT/TBACT for photoresist operations (Page 149A.2.1.1) and solvent cleaning operations (Page 149A.2.2.1).

The Workbook specifies the requirements for commonly permitted sources and is intended to be used as a guide. BACT and TBACT determinations are made or confirmed each time BACT or TBACT requirement are triggered.

III. EMISSIONS

A. Background

Semiconductor manufacturing operations may generate each of the regulated classes of air pollutants: nitrogen oxides (NOx), sulfur dioxide (SO_2), precursor organic compounds (POCs), non-precursor organic compounds (NPOCs), particulate matter smaller than 10 microns in diameter (PM_{10}) and carbon monoxide (CO), as well as a variety of hazardous air pollutants (HAPs) and other toxic compounds, as summarized below:

Pollutant	*Source*
NO_X	1. Combustion of fuel at abatement devices
POC, NPOC	1. Evaporation of wipe cleaning solvents 2. Evaporation of solvent station solvents 3. Evaporation of wafer coating solvents 4. Evaporation of developer/stripper solvents 5. Drying/curing of wafer coatings 6. Combustion of fuel at abatement devices
PM_{10}	1. Aerosols from fuming/agitated wet chemical station chemicals 2. Combustion of fuel at abatement devices
CO / SO_2	Combustion of fuel at abatement devices
HAPs	1. POC, NPOC and PM_{10} emissions may also be HAPs 2. Reactive gas emissions from gaseous operations may be HAPs 3. Metal emissions from sputtering operations may be HAPs

B. Calculation Methods

Emissions may be calculated either by periodic mass balance, by applying an emission factor derived from a process-specific source test, or by applying a generic emission factor.

Periodic mass balances provide the most accurate emissions estimates and should be used whenever possible (Reference 3). Mass balance emission calculations require more records than other methods and may not be preferred by applicants for this reason. Also, a mass balance may not be possible for processes which co-mingle waste streams. However, applicants should always be given the option to perform mass balance emission calculations. A mass-balance option is included in the sample permit condition in Section 4.

Process-specific source tests are costly because even identical process equipment may have widely variable emissions at different processing rates or if different process materials are used. Therefore, accurate characterization of an entire fab with process-specific source tests may require that a large number of tests be performed and may require re-tests when process variables change. Also, the high ventilation airflow used in clean room environments typically result in very dilute pollutant concentrations, which may make a source test impractical. Where process-specific emission factors are used, permit conditions should clearly limit the applicability of such factors to appropriate processes.

Generic emission factors are average factors, which are derived from a large number of related processes. Generic factors for solvent stations and for photoresist applicators

were derived in Reference 4. Generic emission factors require the minimum amount of records, although the fact that emissions may be substantially overestimated may increase applicant costs by triggering BACT or other requirements. The source of generic emission factors should be considered whenever they are applied and such factors should only be used where they will provide conservative emission estimates. It should be noted that EPA has not developed emission factors for semiconductor operations in AP-42 ("Compilation of Air Pollution Emission Factors"). No other authoritative emission factors are known to exist. When generic emission factors are used, permit conditions should identify those factors. Below is a summary of recommended emission calculation methods:

Operation (pollutant)	*Emission Calculation Method (in order of highest preference)*
Any material applied at a wafer coating applicator, including coatings, developers, dispensed cleanup solvents, processing solvents (POC, NPOC, HAPs)	1. Periodic Mass balance 2. Generic emission factor of 90% emission of total solvent content of material [NOTE 1]
Wipe cleaning solvent (POC, NPOC, HAPs)	Periodic Mass balance
Solvent station chemicals used at solvent sinks or other solvent stations (POC, NPOC, HAPs)	1. Periodic Mass balance 2. Generic emission factors of 30% of total solvent content of all chemicals [NOTE 1]
Fuel combustion at abatement devices (NOx, POC, CO)	Source test (emission factors from EPA AP-42, Tables 1.4-1 and 1.4-3 may be used as preliminary estimates to issue an A/C)
Fuel combustion at abatement devices (SO_2, PM_{10})	Emission factors from EPA AP-42, Tables 1.4-1 and 1.4-2 (emissions are too low to justify a source test)
Liquid chemicals used at wet chemical stations (PM_{10})	Assume negligible where equipment is abated by a wet scrubber, otherwise estimate with simplified "spill" correlation in Reference 5 as discussed in Reference 6
Liquid chemicals used at wet chemical stations (HAPs)	Assume negligible where equipment is abated by a wet scrubber, otherwise estimate with simplified "spill" correlation in Reference 5 as discussed in Reference 6
Gases from dry etching, layering (CVD, epitaxial growth), doping (ion implant) (HAPs)	Periodic Mass balance [NOTE 2]
Sputtered metals (HAPs)	Periodic Mass balance [NOTE 2]

Notes: (see next page)

Notes: (continued)

1. Reference 1.

2. Emissions of gases and metals, which are HAPs, should be calculated in the most conservative manner possible. As a first estimate, emissions should be assumed to be equal to total gross usage amounts and compared to risk screening trigger levels in Regulation 2, Rule 1. For those materials where the trigger levels are exceeded, either a risk screening should be performed to verify an insignificant risk, or else a more refined second estimate should be made which takes into account abatement efficiency, etc. This process should be repeated until an insignificant toxic risk is established or the emission estimate has been refined as much as possible.

   It should be noted that Santa Clara County, where many semiconductor fabrication facilities are located, has adopted a “toxic gas ordinance” (Reference 5) which is intended to minimize the impact of accidental releases of toxic gases. Accidental releases are beyond the scope of authority of the District Permit Services Division, although they may result in District enforcement action. The toxic gas ordinance does not apply to normal process emissions, which the ordinance presumably intends to be regulated directly by the District or other agencies. Therefore, it should be assumed that a municipality or other local authority would require the use of gas scrubbers or other control equipment at process gas emission points.

IV. APPLICATION PROCEDURES

District permit application procedures are discussed in the Permit Handbook Chapter entitled “General District Permit Requirements and Permit Application Procedures.” This section discusses application procedures specific to semiconductor manufacturing operations.

Equipment and operations which require permits at "blank wafer manufacturing facilities" and at "assembly and packaging operations" (discussed in Section 1 of this document and listed in Table 1 and Table 3) are permitted in the standard way, without grouping into a "fab area" source. Equipment and operations which require permits at "semiconductor fabrication facilities" (discussed in Section 1 of this document and listed in Table 2) should be grouped into "fab area" sources. Section 2 of this document provides more guidance on fab area permits.

A. Forms

1. General Application Forms

For each permit application, one of the following is required:

- **Form P-101A**: Accelerated Permitting Certification, if eligible in accordance with Regulation 2-1-106, or
- **Form P-101B**: Application for Authority to Construct, Permit to Operate, and Banking

Applications for semiconductor manufacturing facilities should be submitted on the standard permit application form (Form P-101B).

2. Equipment Specific Data Forms

Data form "F" Worksheet is used for "fab area" sources. Data form "G" is used for non-solvent cleaning sources at "blank wafer manufacturing facilities" and at "assembly and packaging operations" while form "S" is used for wipe cleaning and other solvent-cleaning sources at these facilities.

The current version of data Form "F" Worksheet is dated March, 2000. The form should be completed to indicate maximum, annual throughput quantities because these throughput quantities will be identified in the permit condition conditions for the source.

B. Fees

Regulation 3 requires payment of fees for permit applications including a filing fee, an initial fee, and a permit to operate fees. Late fees and retroactive permit fees may be charged for sources constructed or operated without appropriate District permits. Toxic Air Contaminant (TAC) surcharges may also apply to sources using or emitting certain highly toxic substances. The "fab area" source is subject to the fees in Schedule H of Regulation 3. Non-"fab area" sources are subject to the other applicable fee schedules in Regulation 3.

V. ENGINEERING EVALUATION TEMPLATE

This section contains a template for an engineering evaluation of a permit application for the semiconductor fabrication industry. The template provided here is not intended to prescribe the exact format for an evaluation, but to identify the important technical and regulatory elements of an evaluation.

A. EVALUATION REPORT

1. Background

This section should identify all modified existing sources and describe their modifications as well as all new sources. When sources are modified, existing permit conditions should be noted and copies of these conditions should be attached to the evaluation, unless "underline and strikeout" format is used for the modified conditions.

2. Emission Calculations (Annual)

Annual emissions (or increased annual emissions for modified sources) are calculated for each class of regulated pollutants for all sources to establish the emission increase for the application, which is reported below as the "cumulative increase." The cumulative increase is also the basis for calculating required offsets when this requirement is applicable. Annual emissions of HAPs are the basis for determining if the resulting toxic risk is significant or insignificant.

Recommended emission factors for semiconductor manufacturing operations are provided in Section 3.B. Each of the potential emission sources described in Section 3 should be considered.

Spreadsheets are very useful for estimating semiconductor fabrication emissions since a large number of process materials may need to be calculated. One possible format (partial) is as follows:

POC Solvents

Material Description	*Throughput (gals/yr)*	*Density (lb/gal)*	*Emission Factor (%)*	*Unabated POC (lb/yr)*	*Control Eff. (%)*	*Abated POC (lb/yr)*
{Solvent 1}						
{Solvent 2}						
{Solvent 3}						
Subtotal						

NPOC Solvents

Material Description	*Throughput (gals/yr)*	*Density (lb/gal)*	*Emission Factor (%)*	*Unabated POC (lb/yr)*	*Control Eff. (%)*	*Abated POC (lb/yr)*
{Solvent 1}						
{Solvent 2}						
{Solvent 3}						
Subtotal						

Photoresist Maskants, Organic Developers, and Other Coatings

Material Description	*Throughput (gals/yr)*	*Density (lb/gal)*	*Emission Factor (%)*	*Unabated POC (lb/yr)*	*Control Eff. (%)*	*Abated POC (lb/yr)*
{Material 1}						
{Material 2}						
{Material 3}						
Subtotal						

Emission Calculations (Daily):

Daily emissions of each class of regulated pollutants are calculated for each source to establish if the requirement for BACT is triggered. Daily emissions are generally difficult to establish directly because daily records will often not be maintained. Therefore, "daily average" emissions (annual emissions divided by the number of operating days) should be considered as a first estimate. If daily average emissions exceed the daily BACT trigger level or are just below the trigger level (within 20%), it may be assumed that the source will trigger BACT. However, if the applicant is committed to not exceeding BACT trigger levels, daily or weekly records, as appropriate to estimate daily emissions with reasonable certainty, should be imposed to enforce the BACT trigger level. If daily average emissions are more than 20% lower than the BACT trigger level at a production fab area, it may be assumed that BACT will not be triggered, unless other information (such as an infrequent or irregular operating schedule) suggests otherwise.

Research and development (R&D) semiconductor fabrication areas are quite common and these may have a much less consistent operating schedule than a production fab area. The number of annual operating days for R&D fab areas is especially critical when daily emissions are estimated based on annual emissions.

3. Cumulative Increase

The cumulative increase is a summary of the permitted increase of each class of regulated air pollutants.

4. Toxic Risk

As noted in Section 3, HAPs may be produced by a variety of operations related to semiconductor manufacturing. This section should list the emitted quantities of all materials listed in Table 2-1-316 of Regulation 2, Rule 1, indicate if a risk screening was required and performed, as well as the results.

5. Statement of Compliance

a. The requirements of all applicable District regulations (including those which specify source design and operating requirements or emission limits and those which require modeling or public notice or other administrative actions), as well as NSPS and NESHAP standards, should be described, as well as the manner in which the new or modified source complies with these regulations.

b. The status and disposition of the application with regard to CEQA should be described.

c. The status and disposition of the application with regard to Regulation 2-2-413 (school public notice) should be discussed.

d. The status of the application with regard to offset requirements should be discussed. If offsets were required, the source of the offsets should be identified. If offsets were provided through a contemporaneous emission reduction, all of the steps which were used to determine the available credit should be described in detail.

e. The status of all sources with regard to BACT should be discussed. If BACT is triggered, the source of the BACT determination should be identified. If a new determination is made, the process behind the determination should be described.

BACT measures and cost effectiveness criteria are described in Reference 1. Because semiconductor fab areas are permitted as a single source, all fab area emissions are considered together to determine if BACT is triggered for each class of regulated pollutants. However, if BACT is triggered and a cost effectiveness study is performed in accordance with Reference 7, then the cost of abating individual elements of the fab area may be considered. For example, if a fab area is required to abate solvent stations and wafer coating applicators with add-on controls, it may be determined that wipe cleaning within the fab or some specific solvent station may not be cost-effectively abated and therefore do not require add-on controls.

When add-on controls are imposed as BACT, collection efficiency of the controls should always be specified. As a default, 100% collection efficiency should be required, and this may be demonstrated with compliance with the EPA "total enclosure" criteria (Reference 8). Actual measurement of a collection efficiency which does not meet this criteria will not be possible in most cases. Therefore, where this criteria is not satisfied, an inspection of the equipment in question and appropriate permit conditions may be required to establish that collection efficiency is maximized.

Because fab areas often produce very dilute emission streams, thermal and catalytic oxidizers with upstream concentrator sections are commonly used to minimize equipment size and fuel requirements. Where a concentrator is used, permit conditions should clearly note that required abatement efficiencies are "overall" efficiencies which take into account any emissions which are not adsorbed onto the concentrator material and which completely bypass the combustion section. Also, rotary concentrators may be susceptible to seal leaks. It may be appropriate to impose a fugitive emission limit on the seals.

6. Sample Permit Conditions

The purpose of these sample conditions is to illustrate a standard permit condition format and to identify elements, which should be included, and items, which should be addressed in a typical set of, permit conditions. All of the quantities, equipment counts, source test and monitoring schedules and abatement device operating requirements in this set of sample conditions are merely examples and do not represent limits which should automatically be imposed in an actual evaluation. Any allowances, in terms of throughput or emissions, are also merely examples; allowances in an actual evaluation must satisfy the requirements of all applicable regulations.

Boxed text is for information only and should not be included in actual permit conditions.

Conditions for S-xx:

It is helpful to list all of the permitted elements of the fab area and their abatement configuration in the permit conditions so that the permitted configuration is always clear.

1. Equipment in the S-xx fab area shall be abated by the following abatement devices:

   All coating applicators (including photoresist, spin-on-glass and other coatings) shall be abated by A-x.

   All photoresist developers using non-exempt developer solution (where exempt developer solution is any solution which contains less than 10% VOC by weight if unheated, or less than 2.5% by weight if heated) shall be abated by A-x.

   All solvent stations shall be abated by A-x.

   All vapor solvent shall be abated by A-x.

   All wet chemical stations shall be abated by A-x.

   [basis: Cumulative Increase]

If permit condition limits are based on generic or specific emission factors, then emission limits will be in the form of throughput limits. The throughput basis, gross or net - as preferred by the applicant, should be clearly specified.

2. Gross throughput of coatings and related solvents at S-xx coating applicators shall not exceed the following amounts in any consecutive 12-month period:

positive photoresist	x gallons (less than x% VOC by wt)
spin-on-glass	x gallons (less than x% VOC by wt)
HMDS	x gallons
edge bead remover	x gallons (less than x% VOC by wt)
IPA	x gallons (excluding manual wipe cleaning)

Gross throughput of solvents at S-xx solvent stations shall not exceed the following amounts in any consecutive 12 month period:

acetone	x gallons
IPA	x gallons
methanol	x gallons
ethylene glycol	x gallons
photoresist stripper	x gallons (Brands x, y, z OR not to exceed x% VOC by weight)

[basis: Cumulative Increase]

If the fab does not agree to keep separate IPA usage total for wipe cleaning, wafer coating dispensers and solvent stations, each of which will typically have a different emission factor, then emission calculations should assume that the highest factor (100% for wipe cleaning) applies to all IPA use and then impose a single total IPA use limit instead of separate limits.

Net usage of wipe cleaning solvent throughout the S-xx fab shall not exceed the following amounts in any consecutive 12 month period:

IPA	x gallons

Coatings, solvents and other materials other than those listed above shall be used only with the written approval of the District. [basis: Cumulative Increase]

If permit condition limits are based on a mass balance, then emission limits will be in the form of a total emission limit for POC and NPOC compounds. The calculation method / emission factor to be used for each process should be clearly noted. As noted above, these emissions factors are merely examples and should not automatically be applied in an actual permit; the emission calculation methods described in Section 3 should all be considered and the most appropriate used for each fab area.

3. Total emissions of POC and NPOC compounds at S-xx shall not exceed the following amounts in any consecutive 12-month period:

POC	x tons
NPOC	x tons

The following emission factors shall be used:

all materials applied at wafer coating applicators	90% of gross solvent in each material
all materials applied at solvent stations	30% of gross solvent in each material
all wipe cleaning solvents	100% of net solvent usage

Collection and abatement efficiencies used in calculations shall be those which are required for each abatement device in these permit conditions. [basis: Cumulative Increase]

As described in Section 3, in most cases wet chemical stations, gaseous wafer processes and sputterers will not have explicit throughput or emission limits. Many of these processes will be exempt if it is established that associated toxic emissions are not significant.

4. All emissions from the following devices shall be abated as shown:

all wipe cleaning solvents	abated at A-x
wet chemical stations	abated at A-x

dry etching, layering, doping	abated at A-x
sputterers	abated at A-x

[basis: Cumulative Increase]

Abatement devices are subject to RACT, when they exceed BACT trigger levels, in accordance with Regulation 2-2-112.

5. The following emission rates shall not be exceeded at A-x under any operating conditions:

NO_X	x lb/million BTU fuel consumed
CO	x lb/million BTU fuel consumed

[basis: Cumulative Increase]

Each abatement device which is cited in the permit conditions should have operating requirements to ensure that the appropriate abatement efficiency is maintained; if "standard" permit conditions have been developed for a particular abatement technology, the most current version should be used.

Abatement device collection efficiency should always be specified. Typically, 100% collection efficiency should be required, and this may be demonstrated with compliance with the EPA "total enclosure" criteria (Reference 8).

Source tests should be required for POC / NPOC abatement devices. Catalytic oxidizers and oxidizers with concentrator sections are susceptible to maintenance problems (catalyst blinding and de-activation, seal leaks) which do not affect thermal oxidizers and which could degrade performance over time; these units should have periodic source test requirements in addition to an initial source test. All oxidizers should have a minimum operating temperature requirement and a requirement for continuous temperature monitoring.

Source tests may be required for wet scrubbers and other abatement devices if a specific emission limit has been imposed on the abated emissions.

6. The A-x catalytic oxidizer shall comply with one of the following NMHC emission concentration or overall destruction efficiencies. Overall means that the calculated destruction efficiency shall take into account any NMHC compounds which are not collected by the A-x concentrator stage and which are not treated at the A-x combustion stage.

   a. outlet NMHC concentration of 10 ppmv or less measured directly at the A-x combustion stage outlet before the exhaust stream is diluted with the stripped concentrator airstream.

   b. NMHC destruction efficiency greater than 98.5% if NMHC concentration at concentrator outlet is greater than or equal to 2,000 ppmv.

   c. NMHC destruction efficiency greater than 97% if NMHC concentration at concentrator outlet is greater than or equal to 200 ppmv and less than 2,000 ppmv.

d. NMHC destruction efficiency greater than 90% if NMHC concentration at concentrator outlet is less than 200 ppmv.

[basis: BACT; Cumulative Increase]

A Permanent Total Enclosure (PTE) shall be assumed to have a collection efficiency of 100%, according to EPA Method 204. If a fab area enclosure does not have any Natural Draft Openings (NDOs) and all the emissions are ducted to a control device (i.e. no fugitive exhaust points), then the enclosure would meet the criteria for a PTE.

According to EPA, NDOs are defined as "any permanent opening in the enclosure that remains open during operation of the facility and is not connected to a duct in which a fan is installed." Since the doors of a semiconductor fab are only opened to allow personnel in the semiconductor fab (enclosure) and then are closed, such doors are not considered NDOs. Having no NDOs does mean that the semiconductor fab would meet Method 204 criteria for a Temporary Total Enclosure (TTE). If all the emissions of the TTE (semiconductor fab) are ducted to a control device (i.e. no fugitive exhaust points) then the enclosure would meet the criteria for a PTE.

7. A-x shall provide a 100% collection efficiency at all abated equipment and operations, which may be demonstrated by compliance with U.S. EPA Method 204. [basis: Cumulative Increase]

8. A-x shall operate at an average combustion stage temperature of no less than x degrees F, averaged over any 3-minute period. A-x shall be provided with a District-approved continuous temperature monitoring and recording system. [basis: Cumulative Increase]

9. No later than 60 days following the startup of A-x, and thereafter at 24 month intervals, a source test shall be performed on A-x to verify compliance with the outlet concentration/destruction efficiency requirement of CONDITION 6 and the NOx and CO emission rate limits of CONDITION 5. Also, no later than 60 days following startup of A-x, collection efficiency at all sources abated at A-x shall be established to verify compliance with CONDITION 7; collection efficiency need not be re-verified after the initial demonstration.

   Prior to the performance of the source test, the District Source Test Manager shall approve the test procedure. Written notification of the data and time of the test shall be provided to the District Source Test Manager at least 7 days before the performance of the test.

   A copy of the source test results shall be provided to the District within 60 days of the completion of the test. [basis: Cumulative Increase]

Recordkeeping requirements shall reflect whether the fab area has throughput limits or emission limits.

10. Monthly records of the following shall be kept in a District-approved log for at least two years and shall be made available to the District upon request:

a. Type and gross usage of wafer coatings, wafer solvents applied at wafer coating applicators, and solvents used at solvent stations at S-x.

b. Type and net amount of wipe cleaning solvents used throughout S-x.

c. Resulting POC and NPOC emissions, calculated in accordance with CONDITION 2 [where emission limits are used].

[basis: Cumulative Increase]

11. Continuous records of A-x operating temperatures shall be kept in a District-approved log for at least two years and shall be made available to the District upon request. [basis: Cumulative Increase]

7. Recommendations

The evaluation should conclude with a description of sources addressed in the evaluation and the permit actions, which are appropriate for each. For example, the following source description may be used:

S-X Semiconductor Fabrication Area

VI. APPENDIX

A. REFERENCES

1. Bay Area Air Quality Management District, "BACT/TBACT Workbook," June 1995.

2. Bay Area Air Quality Management District, Hill, S. "Emissions from Semiconductor Manufacturing in the Bay Area"; April 1987.

3. Halloway, P., McGuire, G.; "Handbook of Compound Semiconductors;" Noyes Publications, 1995.

4. Higgs, T.; "Emissions Estimates for a Semiconductor Manufacturing Facility," presented at Air & Waste Management Association conference, September 1996, New Orleans.

5. Santa Clara County Fire Chief’s Association, Toxic Gas Model Ordinance, June 29, 1997.

6. Sax, N., Lewis, R.; "Hawley's Condensed Chemical Dictionary"; eleventh edition; Van Nostrand Reinhold, 1987.

7. U. S. Environmental Protection Agency; "Estimating Releases and Waste Treatment Efficiencies for the Toxic Chemical Release and Inventory Form," EPA 560/4-88-002, 1987, p. 6-4.

8. U. S. Environmental Protection Agency; Method 204: "Criteria for and Verification of a Permanent or Temporary Total Enclosure."

9. U. S. Environmental Protection Agency; "Preferred and Alternative Methods for Estimating Air Emissions from Semiconductor Manufacturing," Review Draft, April 1997.

10. U. S. Environmental Protection Agency, Electronic Mail from Candace Sorrell, February 2, 1998.

A. GLOSSARY

Best Available Control Technology / BACT: A requirement to establish and to require use of "best available" abatement technology for regulated pollutants as described in Regulation 2, Rule 2; a specific abatement technology which complies with Regulation 2, Rule 2, possibly listed in Reference 7.

Blank Wafer Production: All processes related to the production of finished blank wafers.

Hazardous Air Pollutant / HAP: In the context of a "major facility" permit evaluation (described in Regulation 2, Rule 6), a HAP is any compound listed in the Federal Clean Air Act, Title V, Section 112(b); in the context of a non-major facility permit evaluation, a HAP is any compound with an assigned risk screening trigger level in Table 2-1-316 of Regulation 2, Rule 1.

Hexamethyldisilazane/ HMDS: Chemical used in photoresist applicators.

Integrated Circuit / IC: A miniaturized electronic circuit produced on or in a wafer of silicon or other crystalline material.

Non-Methane Hydrocarbon/ NMHC: All hydrocarbons, excluding methane.

Propylene Glycol Methyl Ether Acetate/ PGMEA: Chemical used in solvent stations.

Packaging and Assembly: All processes related to the conversion of completed semiconductor wafers into components suitable for assembly onto a printed circuit board.

Semiconductor Manufacturing: All processes related to the production of packaged semiconductor electronic products beginning with the manufacture of blank wafers, up to, but excluding, assembly of printed circuit boards.

Semiconductor Fabrication: All processes related to the production of integrated circuits on blank wafers, up to, but excluding, the division of a completed wafer into individual integrated circuits. In accordance with Regulation 2-1-231, semiconductor fabrication does not include crystal growth, circuit separation and encapsulation operations.

Semiconductor Fabrication Area / Fab Area: A grouping of equipment and operations used in semiconductor fabrication as a single permitted source.